



SHEET 1 OF 1



INFORMATION DISCLOSURE CITATION PTO-1449	CUSTOMER NUMBER 26615	ATTORNEY'S DKT No. H1477	APPLICATION No. 10/614,052				
		APPLICANT(S) Shibly S. AHMED et al.					
		FILING DATE July 8, 2003	GROUP 2812				
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
WLL	Copy of U.S. Serial No. 10/699,887; filed November 4, 2003; entitled: "SELF ALIGNED DAMASCENE GATE," 35 pages.						
EXAMINER				DATE CONSIDERED 5/6/2004			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).



INFORMATION DISCLOSURE CITATION PTO-1449		Customer Number 26615	ATTORNEY'S DKT No. H1477		APPLICATION No. 10/614,052		
			APPLICANT(S) Shibly S. Ahmed et al.				
			FILING DATE July 8, 2003		GROUP 2812		
U.S. PATENT DOCUMENTS							
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FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
WL	Co-pending U.S. Application Serial No. 10/348,910 filed January 23, 2003 entitled: "Narrow Fin FinFet," 16 page specification, 13 sheets of drawings.						
EXAMINER Wald L. Lusk Jr.				DATE CONSIDERED 5/6/2004			

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INFORMATION DISCLOSURE CITATION PTO-1449		 26615 <small>PATENT TRADEMARK OFFICE</small>		ATTORNEY'S DKT No. H1477 APPLICANT(S) Shibly S. AHMED et al. FILING DATE July 8, 2003		APPLICATION No. Unassigned GROUP Unassigned	
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FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
WL	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.						
WL	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.						
WL	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.						
WL	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.						
WL	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.						
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